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A STUDY OF THE EFFECT OF ADDITIONAL INEQUALITIES IN INTEGER PROGRAMMING FOR LOGICAL DESIGN

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This work is dedicated to my wife and son.

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1. INTRODUCTION

Logical design by integer programming has proved to be an efficient approach to finding optimal networks [10, 11, 12]. Several computer programs for the logical design of optimal networks by integer programming techniques have been prepared at the University of Illinois.

This work is concerned with computer programs based on the implicit enumeration method, and inequalities added to the integer programming problem, in order to speed-up the execution time. These additional inequalities, based on intrinsic properties of the networks, are incorporated in the inequalities for the integer programming logical design.

The objective of the present work is to establish how effective these additional inequalities are in reducing the execution time of the mentioned programs for several cases of network design.

2. PROBLEM STATEMENT

It is assumed that the reader is familiar with integer linear programming or that he can easily refer to available publications in that field [10, 11, 12, 13].

Integer linear programming techniques have been implemented by computer programs to solve the optimal design problem for logical networks. The implicit enumeration method based on inequalities is used at the University of Illinois after computational experiences with logical design. Description of the algorithm used is available in the literature [1, 6, 11, 12, 13].

As previously stated, the inclusion of additional inequalities based on some features of gates and networks is found to speed-up the execution time of the computer programs [1, 10, 11].

In what follows, it will be determined to what extent each type of additional inequality effects the computation time for the following cases of logical design:

(i) - Networks with three input variables and five NOR gates.

(ii) - Networks with three input variables and six NOR gates.

(iii) - Networks with three input variables and seven NOR gates.

(iv) - Networks with four input variables and five NOR gates.

(v) - Networks with four input variables and six NOR gates.

(vi) - Networks with four input variables and seven NOR gates.

(vii) - Networks with three input variables and five NOR or NAND gates(i.e., each network consists of a mixture of NOR and NAND gates).

(viii) - Networks with four input variables and five AND or OR gates(i.e., each network consists of a mixture of AND or OR gates)..

(ix) - One-bit adder networks with three input variables and eight NOR gates.

For all cases the all-interconnection formulation was used. In addition, the feed-forward formulation was used for cases (i) and (ii) under several combinations of types of additional inequalities.

The following assumptions are made in the present work:

(1) Complemented input variables are not available, i.e., the so-called "single rail logic" is assumed for NOR, NOR-AND and NOR-NAND design cases. But both complemented and non-complemented input variables are available in the AND-OR design case.

(2) No fan-in or fan-out restrictions are considered (although they can be included in the programs used).

(3) The number of levels for the implementation of the networks is not restricted (though the programs permit this restriction to be included).

(4) Except for the one-bit adder design case, the number of outputs of the networks is limited to one (although the programs, again, permit multiple outputs).

Let us show the additional inequalities for the logical design cases of interest in this paper.

First we need some notation conventions in order to understand the formulas which appear below.

Variables are needed to represent : a) the external variables which are inputs to the network gate; b) whether or not an external variable connects to a gate (G); c) whether or not a gate (G_i) connects to another gate (G_j), and d) the type of the gate when more than one type is involved.

In the given order, these variables are:

a) $x_1, x_2, \ldots, x_n$ represent n uncomplemented variables (or simply variables) which can be external input variables. Also, $\bar{x}_1, \bar{x}_2, \ldots, \bar{x}_n$ represent the corresponding complemented variables.

b) v_{ij} is a <u>connection</u> from the i-th external variable, x_i, to the j-th gate, G_j; v_{ij} can take on the values given by:

$$v_{ij} = \begin{cases} 1 \text{ if the connection exists} \\ 0 \text{ if the connection does not exist.} \end{cases}$$

$\bar{v}_{ij}$ will represent in similar way connections from complemented variables to gates.

c) α_{ij} represents the <u>interconnection</u> from gate G_i to gate G_j, and its value will be:

$$\alpha_{ij} = \begin{cases} 1 \text{ if the interconnection exists} \\ 0 \text{ if the interconnection does not exist.} \end{cases}$$

d) As we are concerned with at most two different types of gates in the logical design of networks with a mixture of types of gates, λ_j will represent the type of gate j. λ_j will take values as given by:

i - in the case of networks with a mixture of NOR and NAND gates

$$\lambda_j = \begin{cases} 1 \text{ if the gate is NOR} \\ 0 \text{ if the gate is NAND} \end{cases}$$

ii - in the case of networks with a mixture of OR and AND gates

$$\lambda_j = \begin{cases} 1 \text{ if the gate is OR} \\ 0 \text{ if the gate is AND} \end{cases}$$

and

iii - in the case of a network with a mixture or NOR and AND gates

$$\lambda_j = \begin{cases} 1 \text{ if the gate is NOR} \\ 0 \text{ if the gate is AND} \end{cases}$$

In what follows, formulas are given without deduction, which can be found elsewhere [1, 12, 13].

For logical networks using NOR gates we can establish five types of additional inequalities (from now on let us refer to them simply as "inequalities"):

Type 1 - Each gate must have at least two input* interconnections or at least one input connection. This condition can be expressed by the inequalities:

$$\sum_{i=1}^{j-1} \alpha_{ij} + 2 \sum_{i=1}^{n} v_{ij} \geq 2 \quad j = 1,2,\ldots, R-1 \text{ for f.f.f.}^{**}$$

and

$$\sum_{\substack{i=1 \\ i \neq j}}^{R} \alpha_{ij} + 2 \sum_{i=1}^{n} v_{ij} \geq 2 \quad j = 1,2,\ldots, R-1 \text{ for a.i.f.}$$

Type 2 - Every gate (except for the output gate) must have at least one output interconnection to another gate in the network. This is an obvious condition in order to have the gate within the network, and can be expressed by the inequalities:

$$\sum_{j=i+1}^{R} \alpha_{ij} \geq 1 \quad i = 1,2,\ldots, R-1 \text{ for f.f.f.}$$

and

$$\sum_{\substack{j=1 \\ j \neq i}}^{R} \alpha_{ij} \geq 1 \quad i = 1,2,\ldots, R-1 \text{ for a.i.f.}$$

---

* For the sake of simplicity, let an input be defined as a connection from an external variable to a gate or an interconnection from one gate to another; the words connection or interconnection will be added, as qualifiers, to the word input when the distinction between the two types inputs is necessary.

** For the formulas about inequalities, f.f.f. stands for feed-forward formulation and a.i.f. for all-interconnection formulation. The gates are numbered from 1 to R; G_R being the output gate. For details about f.f.f. and a.i.f. see [1, 10]. As a convention, summations Σ are assumed to be set to zero, if the upper limit takes values less than the lower limit.

Type 3 - A gate which is interconnected to the output gate is not interconnected to any other gate. The corresponding inequalities are:

$$U\,(1 - \alpha_{iR}) \geq \sum_{j=i+1}^{R-1} \alpha_{ij} \qquad i = 1,2,\ldots, R-2 \text{ for f.f.f.}$$

and $$U\,(1 - \alpha_{iR}) \geq \sum_{\substack{j=1 \\ j\neq i}}^{R-1} \alpha_{ij} \qquad i = 1,2,\ldots, R-1 \text{ for a.i.f.}$$

where U is a positive number, large enough so that the inequalities become non-restrictive if $\alpha_{iR} = 0$.

Type 4 - For the structure shown in fig. 1 the network is not optimal if $\alpha_{ij} = \alpha_{ik} = \alpha_{jk} = 1$, and if gate G_j has no other output interconnection. This condition, usually referred to as the <u>triangular condition</u>, is expressed by:

$$\sum_{\substack{\ell=j+1 \\ \ell\neq k}}^{R} \alpha_{j\ell} + 2 \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk}$$

$i = 1,2,\ldots, R-2$

$j = i + 1, 2,\ldots, R-1$

$k = j + 1, 2,\ldots, R$

for f.f.f.

$$\sum_{\substack{\ell=1 \\ \ell\neq j \\ \ell\neq k}}^{R} \alpha_{j\ell} + 2 \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk}$$

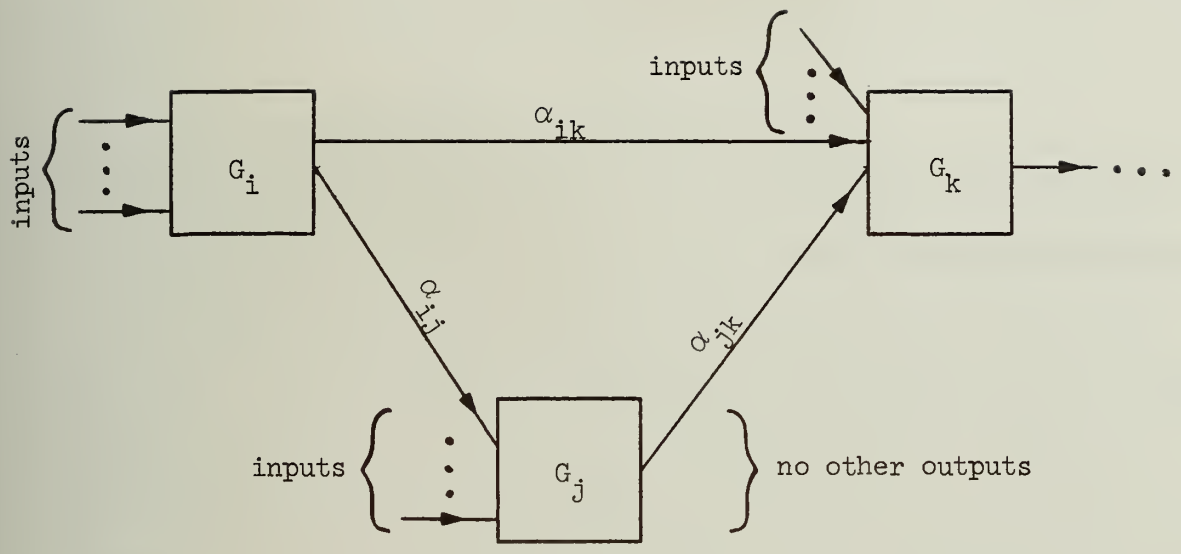
$i = 1,2,\ldots, R$

$j = 1,2,\ldots, R$

$k = 1,2,\ldots, R$

$i \neq j \neq k$

for a.i.f.



Type 5 - This inequality type is the triangular condition with gate G_i in fig. 1, replaced by an external variable x_i. Then we have:

$$\sum_{\substack{\ell=j+1 \\ \ell \neq k}}^{R} \alpha_{j\ell} + 2 \geq v_{ij} + v_{ik} + \alpha_{jk}$$

$j = 1,2,\ldots, R-1$

$k = j+1,2,\ldots, R$

$i = 1,2,\ldots, n$

for f.f.f.

$$\sum_{\substack{\ell=1 \\ \ell\neq j \\ \ell\neq k}}^{R} \alpha_{j\ell} + 2 \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad \begin{array}{l} j = 1,2,\ldots, R \\ k = 1,2,\ldots, R \\ i = 1,2,\ldots, n \\ j \neq k \\ \text{for a.i.f.} \end{array}$$

All inequalities described in the following refer to the all interconnection formulation only.

For the NOR-AND design case the following inequalities apply:

Type 6 - This inequality is a replacement for inequality type 1 of the NOR design case, and it takes into account the two different types of gates we now have. The inequality establishes the condition that every AND gate must have at least two inputs, while a NOR gate must have at least one.

Then:

$$\sum_{i=1}^{n} v_{ij} + \sum_{\substack{i=1 \\ i\neq j}}^{R} \alpha_{ij} \geq 2 - \lambda_j \qquad j = 1,2,\ldots, R$$

$$\text{where } \lambda_j = \begin{cases} 1 \text{ for a NOR gate} \\ 0 \text{ for an AND gate} \end{cases}$$

The NOR-AND design case includes two more sets of triangular conditions similar to those for inequalities types 4 and 5 of the NOR design case; these inequalities are:

Type 7 - If either gate G_j or gate G_k in the triangular condition (see fig. 1) is an AND gate, the triangular condition still holds, even if G_j interconnects to other gates different from G_k. In terms of inequalities:

$$\lambda_k + 2 \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk} \qquad i = 1,2,\ldots, R^{*}$$

$$j = 1,2,\ldots, R$$

and $$\lambda_j + 2 \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk} \qquad k = 1,2,\ldots, R$$

for $i \neq j \neq k$ and λ as previously defined.

Type 8 - In inequality type 7 gate G_i can be replaced by a connection from an external variable and the triangular condition still holds; the inequalities expressing this are:

$$\lambda_k + 2 \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad j = 1,2,\ldots, R^{**}$$

$$k = 1,2,\ldots, R$$

$$\lambda_j + 2 \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad i = 1,2,\ldots, n$$

$$j \neq k$$

Besides inequality types 6, 7 and 8, for NOR-AND design case inequality types 2 through 5 of the NOR design case still hold. The same is true for the NOR-NAND design case but the presence of a new type of gate, NAND, brings in the following four new types of inequalities:

Type 9 - Each gate has at least one input connection or interconnection. The corresponding inequality is:

$$\sum_{i=1} v_{ij} + \sum_{\substack{i=1 \\ i \neq j}} \alpha_{ij} \geq 1 \qquad j = 1,2,\ldots, R$$

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* See Appendix B for programming details.

** See Appendix B.

There is another type of triangular condition for NOR-NAND design case as follows:

Type 10 - This inequality implies that if gates G_j and G_k in the triangular condition <u>are of different type</u>, then the triangular condition (see fig. 1) holds even if gate G_j interconnects tc gates other than G_k, i.e. :

$$2 + (1 - \lambda_j) + \lambda_k \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk} \qquad i = 1,2,\ldots, R^*$$

$$j = 1,2,\ldots, R$$

$$2 + (1 - \lambda_k) + \lambda_j \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk} \qquad k = 1,2,\ldots, R$$

$$i \neq j \neq k$$

$$\text{now } \lambda_i = \begin{cases} 1 \text{ for a NOR gate} \\ 0 \text{ for a NAND gate} \end{cases}$$

Type 11 - In inequality type 10 gate G_i can be replaced by an external input. Then:

$$2 + (1 - \lambda_j) + \lambda_k \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad j = 1,2,\ldots, R^{**}$$

$$k = 1,2,\ldots, R$$

$$2 + (1 - \lambda_k) + \lambda_j \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad i = 1,2,\ldots, n$$

$$j \neq k$$

Type 12 - If a gate has only one input, it can be set to a NOR gate:

$$\lambda_j + \sum_{\substack{i=1 \\ i \neq j}}^{R} \alpha_{ij} + \sum_{i=1}^{n} v_{ij} \geq 2 \qquad j = 1,2,\ldots, R$$

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* See Appendix B.

** See Appendix B.

In the case of AND-OR design, inequality types 2 and 3 about input and output conditions for NOR design are still valid, but the other conditions modify to the five following new types of inequalities:

Type 13 - This is again a modification to inequality type 1 according to the types of gates, AND and OR. It states that each gate must have at least two inputs. In terms of inequalities:

$$\sum_{i=1}^{n} v_{ij} + \sum_{\substack{i=1 \\ i\neq j}}^{R} \alpha_{ij} + \sum_{i=1}^{n} \bar{v}_{ij} \geq 2 \qquad j = 1,2,\ldots, R \quad (13)$$

where $\bar{v}_{ij}$ stands for the connection from a complemented variable $\bar{x}_i$ to the gate G_j, as previously defined. This is necessary in AND-OR design since we need a complete set of logical functions to realize a general boolean function [13].

Type 14 - The triangular condition holds even if gate G_j interconnects to one or more gates different from G_k. This is formalized with the expression:

$$2 \geq \alpha_{ij} + \alpha_{ik} + \alpha_{jk} \qquad \begin{array}{l} i = 1,2,\ldots, R \\ j = 1,2,\ldots, R \\ k = 1,2,\ldots, R \\ i \neq j \neq k \end{array}$$

Type 15 - In the triangular condition of inequality type 14 gate G_i can be replaced by an external variable input, complemented or not, then:

$$2 \geq v_{ij} + v_{ik} + \alpha_{jk} \qquad \begin{array}{l} j = 1,2,\ldots, R \\ k = 1,2,\ldots, R \\ i = 1,2,\ldots, n \\ j \neq k \end{array}$$

or

$$2 \geq \bar{v}_{ij} + \bar{v}_{ik} + \alpha_{jk}$$

Type 16 - If gate G_i interconnects to gate G_j and the gates are of the same type(both are AND gates or OR gates), then G_i must have at least one more output interconnection:

$$\sum_{\substack{\ell=1 \\ \ell\neq i \\ \ell\neq j}}^{R} \alpha_{i\ell} + \lambda_i + \lambda_j \geq \alpha_{ij} \qquad \begin{array}{l} i = 1,2,\ldots, R \\ j = 1,2,\ldots, R \\ i \neq j \end{array}$$

$$\sum_{\substack{\ell=1 \\ \ell\neq i \\ \ell\neq j}}^{R} \alpha_{i\ell} + 2 \geq \lambda_i + \lambda_j + \alpha_{ij}$$

$$\text{For AND-OR design} \quad \lambda_i = \begin{cases} 1 \text{ for an OR gate} \\ 0 \text{ for an AND gate} \end{cases}$$

Type 17 - In the network there must be at least one AND gate and at least one OR gate:

$$\sum_{i=1}^{R} \lambda_i \geq 1$$

and

$$R - 1 \geq \sum_{i=1}^{R} \lambda_i$$

The above types of inequalities, type 1 to type 17, are not the only ones that can be established for the logical design cases since some kinds of geometrical symetries and ordering between the gates can be exploited, in order to preclude certain network configurations from being generated during computation. However, only those seventeen types were used in the logical design by integer programming, in order to limit the number of additional inequalities to a reasonable size [1, 7, 8]. See table 1 for the inequalities tested in each design case in this work.

inequality type / design case	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
NOR*	x	x	x	x	x												
NOR-AND		x	x	x	x	x	x	x									
NOR-NAND		x	x	x	x				x	x	x	x					
AND-OR		x	0										x	x	0	x	x

x signifies that the inequality type was checked.
0 signifies that the inequality type applies but was not checked.
A blank signifies that the inequality does not apply to the design case.
* includes the case of the one-bit adder design.

Table 1. Additional inequalities which apply and were checked for the logical design case.

For computational purposes two different programs were used: ILLIP (standing for ILLinois Integer Program) for the feed-forward formulation and ILLODIE-AIF (standing for ILlinois LOgical Design Implicit Enumeration using the All-interconnection Inequality Formulation) for the all interconnection formulation. Descriptions of the programs and programming manuals for them are available [5,9], and we will not discuss these programs here.

Computation was arranged in such a way that for every design case and almost all tested functions, the programs were run first with all additional inequalities included, and then with some types of additional inequalities removed. The types of inequalities which were eliminated varied with the different design cases. For some cases (see tables 8 and 9), additional inequalities were all removed for one of the runs, then the different types of inequalities were included individually or in different combinations on subsequent runs. This was done in those cases in which the results removing inequalities were not very conclusive and an additional test appeared to be necessary.

3. COMPUTATIONAL RESULTS AND CONCLUSIONS

For the following design cases we used functions taken from the literature as indicated in Appendix A. The number of functions used in each case was determined from the consideration of computer time cost, though the greater number of functions the more reliable the statistics would be.

3.1 NOR design

3.1.1 NOR design with all-interconnection formulation

a) Table 2., which is a summary of tables A 12., A 13., and A 14. in Appendix A shows the average computation times for five functions in each of the three tested design cases: with five, six, and seven NOR gates. The all-interconnection program was run first with all additional inequalities included, and then all combinations of additional inequalities were removed, one-by-one and in pairs.

The main purpose of these runs was to determine for the NOR design case if the effect of the additional inequalities when removed in pairs is additive or not.

As can be seen in table 2, the effect of removing inequalities is not additive; it can be observed, however, that the effect of a specific type of inequality when removed alone is in the same direction as when it is removed in combination with some other type of inequality. For example, inequality types 1 and 3 produce the largest execution time figures when individually removed and then, when they are both simultaneously

case	5 gates			6 gates			7 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All inequalities included	1.12	29	14	4.61	132	14	34.60	869	122
All except type 1	1.29	40	16	4.77	128	14	37.72	982	119
All except type 2	1.12	29	14	4.37	132	14	33.94	869	122
All except type 3	1.25	36	19	5.20	163	15	41.50	1120	149
All except type 4	1.11	29	14	4.52	148	14	30.28	1081	122
All except type 5	1.06	29	14	4.24	132	14	32.60	869	122
All except types 1,2	1.39	40	16	4.75	128	14	37.69	982	119
All except types 1,3	1.54	47	19	5.42	172	15	44.45	1204	152
All except types 1,4	1.22	40	16	4.70	170	14	39.23	1214	119
All except types 1,5	1.22	40	16	4.41	128	14	34.69	982	119

Table 2. Three variable NOR design.
(All-interconnection formulation).
(Summary of Tables A 12., A 13., A 14. in Appendix A).

(continued)

case	5 gates			6 gates			7 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All except types 2,3	1.27	36	19	5.13	163	15	41.01	1120	149
All except types 2,4	1.10	29	14	4.32	148	14	36.28	1081	122
All except types 2,5	1.08	29	14	4.22	132	14	32.55	869	122
All except types 3,4	1.20	37	19	5.10	181	15	41.88	1376	150
All except types 3,5	1.22	37	19	4.93	163	15	38.49	1122	149
All except types 4,5	0.98	29	14	3.97	148	14	32.25	1081	122
Maximum of the Averages	1.54	47	19	5.42	181	15	44.45	1376	152
Minimum of the Averages	0.98	29	14	3.97	128	14	32.25	869	119
Number of Functions Tested	5			5			5		

(continued from the previous page)

Table 2. Three variable NOR design.
(All-interconnection formulation).
(Summary of Tables A 12., A 13., A 14. in Appendix A).

removed, they produce the largest execution time of all tested combinations.

In a similar analysis, it can be observed that inequality types 4 and 5 show the smallest figures for execution time in table 2, when they are individually removed, and again their combination, when removed, produces the smallest of all execution times, even smaller than that of the case in which all inequality types were included.

b) Table 3., which is a summary of tables A 1., A 2., A 3. in Appendix A, shows the average computation time for almost all possible functions with three input variables in NOR designs with five gates, and for all the functions with three input variables in NOR design with six and seven gates.

After the non-additivity of the effect of the removal of different inequality types on the computation time was established, as shown in part a), only the removal of individual types of inequalities was considered.

In table 3., it is observed that the largest figures for the average of the execution time in the cases of five, six seven gates are given by the removal of inequality types 1, 3 and 3 respectively. The second to the largest time is produced by the removal of inequality types 3, 1 and 1, corresponding to the five, six and seven NOR gates design.

This implies that inequality types 1 and 3 are very effecti in reducing execution time when they are present in the program.

case	5 gates			6 gates			7 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All inequalities included	0.97	29	12	5.30	157	32	32.92	821	100
All except type 1	1.20	39	14	5.96	182	41	35.52	920	106
All except type 2	0.98	29	12	5.12	157	32	32.14	821	100
All except type 3	1.05	33	14	6.24	199	42	39.22	1052	131
All except type 4	0.93	29	12	5.20	179	35	34.52	1027	100
All except type 5	0.96	30	13	4.96	158	32	30.93	821	100
Maximum of the Averages	1.20	39	14	6.24	199	42	39.22	1052	131
Minimum of the Averages	0.93	29	12	4.96	157	32	30.93	821	100
Number of Functions Tested	22			15			6		

$\bar{t}$: average computation time in seconds.
$\bar{I}$: average of total number of Iterations for the solution.
$\overline{FO}$: average of number of iterations to obtain First Optimal solution.

Table 3. Three variable NOR design.
(All-interconnection formulation).
(summary of Tables A 1., A 2., and A 3.).

It is also noticed in table 3 that both inequality types 1 and 3 appear to be more effective when the number of gates increases since the differences from the figures for the run in which all inequality types are included become larger as the number of gates is increased.

Inequality types 4 and 5 when removed from the program produce execution time figures which are the smallest for the 5 gate case while inequality type 2 produces almost no effect in computation time. It is observed, however, that when the number of gates increases inequality type 4 becomes more effective in reducing execution time, inequality type 5 instead produces an adverse effect when the number of gates increases but inequality type 2 remains ineffective.

These analyses lead us to conclude that inequality types 1 and 3 should always be included in the program if we want to obtain the minimum execution time. Inequality type 4 should be included for designs with more than 6 gates and inequality types 2 and 5 should be removed since they do not affect execution time (type 2) or affect the execution time adversely (type 5).

Let us check the NOR design with four input variables. In observing table 4 it is noticed that inequality type 3 produces the largest time figures for all number of gates; inequality type 1 is now less effective in reducing execution time than in the case of three variables; and inequality types 2 and 5 have almost no affect on execution time especially for

case	5 gates			6 gates			7 gates		
	$\bar{t}$	$\bar{I}$	$\bar{FO}$	$\bar{t}$	$\bar{I}$	$\bar{FO}$	t	I	FO
All inequalities included	2.22	42	13	31.32	636	42	117.17	2071	448
All except type 1	2.66	54	16	39.88	814	42	119.42	2091	456
All except type 2	2.39	42	13	32.95	636	42	119.49	2071	448
All except type 3	2.68	53	16	44.5	972	81	159.38	2932	684
All except type 4	2.17	42	13	34.16	734	42	133.16	2587	448
All except type 5	2.28	42	13	29.66	636	42	120.70	2327	488
Maximum of the Averages	2.68	54	16	44.5	972	81	159.38	2587	684
Minimum of the Averages	2.17	42	13	29.66	636	42	117.17	2071	448
Number of Functions Tested	10			5			1		

$\bar{t}$: average computation time in seconds.
$\bar{I}$: average of total number of Iteration for the solution.
$\bar{FO}$: average number of iterations to obtain First Optimal solution.

Table 4. Four variable NOR design.
(All-interconnection formulation).
(Summary of Tables A 4., A 5., A 6.).

the case of seven gates. Inequality type 4 shows a similar behavior to the three variable design.

It should be noticed that for seven gates all inequality types are effective in reducing execution time. This tendency appears to show that when the number of gates and the number of variables increases the additional inequalities become more effective regarding execution time.

It can be concluded that inequality types 3 and 4 should always be included in the program if we want to obtain the minimum execution time, and inequality type 5 should be removed from the NOR design case with five and six gates, but probably should be included for designs with more than six gates. Unfortunately, fund limitations for computation time impeded testing of designs with eight or more gates (see [2]) to obtain reliable statistics to confirm the last assertion. Further research in this direction is desirable.

c) In table 5, results are shown for the design of a one-bit full adder with eight NOR gates. It can be observed here that removal of any type of additional inequalities decreases execution time with respect to the case in which all inequality types are included. This appears to show that additional inequalities, in this case, can be removed without increasing execution time. In fact, the name table shows the execution time drastically reduced for the case in which all additional inequalities were removed, in comparison to the case in which all the additional inequalities were included. In addition,

case	t	I	FO
All inequalities included	55.74	1029	16
All except type 1	52.59	1049	16
All except type 2	51.76	1029	16
All except type 3	53.67	1029	16
All except type 4	41.58	1073	16
All except type 5	47.40	1029	16
All inequalities removed	36.64	1081	16
With type 1 only	37.20	1073	16
With type 2 only	35.65	1081	16
With type 3 only	36.16	1081	16
With type 4 only	49.31	1049	16
With type 5 only	40.32	1081	16
Maximum values	55.74	1081	16
Minimum values	35.65	1029	16

$\overline{t}$: time in seconds
$\overline{I}$: total number of iterations to obtain all solutions
$\overline{FO}$: number of iterations to obtain First Optimal Solution

Table 5. Three variable, eight NOR gate, one-bit Full Adder design. (All-interconnection formulation).

it should be noticed that when inequality types 1, 2, and 3 were individually added to the program, the difference with the case of all inequalities removed is very small (addition of inequality type 2 slightly reduces time but judging from the number of iterations, it could be due to timing accuracy of the computer), and that inequality types 4 and 5 produce the worst effect in execution time when included in the program.

3.1.1.1 Summary of conclusions for the NOR design with all interconnection formulation

(i) - It can be said, in general, and according to the results i the previous section, that the inequality type which has the best effect in reducing execution time for single output NOR networks with the all-interconnection formulation is type 3, in both three and four variables cases. It would also be desirable to include types 1 and 4, though they are not always as effective as type 3.

(ii) - Inequality types 2 and 5 could be left out of the program, since they have adverse effect or marginal speed improvement. They might be, however, effective for five or more variables, or for eight or more gates.

Inequalities related to the triangular condition (i.e., types 4 and 5) probably because of the great number of additional inequalities generated, actually increase execution time in some cases. Then additional inequality types 4 and 5 should be removed for the case of five or less NOR gate design but apparently they should be included for cases

of six or more NOR gate designs according to the numerical results discussed above.

Table 6 summarizes the effect of additional inequalities for the NOR design with the all-interconnection formulation program.

case		most effective types	marginally effective types	adversely effective types
3 variable	5 gates	1,3	2	4,5
	6 gates	3,1	2	4,5
	7 gates	3,1,4	2	5
4 variable	5 gates	3,1,2	5	4
	6 gates	3,1,4	2	5
	7 gates	3,4	1,2,5	
one-bit Full adder				4,5,1,3,2

Table 6. Comparison of the effect of additional inequalities on NOR design with all-interconnection formulation.

3.1.2 NOR design with feed-forward formulation

a) - In the case of using the feed-forward formulation program for the NOR design case, table 7, which is a summary of tables A7. and A8. in Appendix A, shows that inequality types 5 and 1 in this order produce the largest execution times when removed from the program, while inequality types 3, 4 and 2, again in the given order, produce the smallest execution times when removed from the design program for five NOR gates. Similarly, in designs with 6 gates, inequality types 1 and 3 give the largest execution times and inequality types 4, 5 and 2 give the smallest ones. Unlike the NOR case with the all-interconnection formulations, all types are effective.

b) - In order to compare the effect on execution time from a different angle, a separate test for ten functions and five gate NOR design, with the feed-forward formulation program, was run (table A 9.). For this test, all additional inequalities were initially removed and then each inequality type was added. Results for this test, (see table 8), which is a summary of table A9. in Appendix A, proved the reduction of execution time given by inequality type 1, followed by inequalit types 2, 5 and 3, decreasing in this order. Inequality type 4 appears to have little effect on the computation time.

c) The results above were confirmed by an additional test, made on two of the functions, one for five NOR gates and one for six NOR gates, as shown in table 9. For this test, the

case	5 gates			6 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All inequalities included	4.26	118	35	62.16	1813	157
All except type 1	5.16	168	53	122.20	4274	293
All except type 2	4.58	137	38	77.42	2158	191
All except type 3	4.48	131	41	78.96	2397	261
All except type 4	4.56	137	37	70.07	2007	222
All except type 5	5.80	171	44	73.04	1992	69
Maximum of the Averages	5.80	171	53	122.20	4274	293
Minimum of the Averages	4.26	118	35	62.16	1813	69
Number of functions tested	22			5		

$\bar{t}$: average computation time in seconds.
$\bar{I}$: average Total number of iterations for the solution.
$\overline{FO}$: average of number of iterations to obtain First Optimal Solution.

Table 7. Three variable NOR design. (Feed-forward formulation). (Summary of Tables A 7. and A 8.)

case	$\overline{t}$	$\overline{I}$	$\overline{FO}$
All inequalities removed	14.24	439	67
With type 1 only	7.44	249	49
With type 2 only	11.28	397	58
With type 3 only	13.69	457	113
With type 4 only	14.62	484	69
With type 5 only	11.61	399	154
Maximum of the Averages	14.62	484	154
Minimum of the Averages	7.44	249	58

Table 8. Three variable, five NOR gate design.
(Feed-forward formulation).
Adding inequalities one-by-one(Summary of Table A 9.)

case	5 gate NOR fun. 37 [4]	6 gate NOR fun. 60 [4]
All inequalities removed	14.73	219.84
With type 4 only	14.48	348.75
With types 4,1 only	7.83	-
With types 4,1,2 only	7.18	-
With types 4,1,2,3 only	5.80	-
With type 1 only	8.39	102.16
All inequalities included	3.72	54.67
Maximum time	14.73	348.75
Minimum time	3.72	54.67

- : case not tested.

Table 9. Three variable, NOR design.
(Test cases for feed-forward formulation).

program was run with all additional inequalities removed first, then adding the other additional inequalities one-by-one in successive runs. In the case of the function for five gates, the weak effect of inequality type 4 on the execution time, and the strong effect of inequality type 4 when added to the program, can be observed. Notice that all inequalities proved to be effective in reducing execution time for that particular function.

For the six-gate function, in the same table (8) it can be observed that inequality type 4 had an adverse effect in execution time (more than 58% time increase). While inequality type 1 showed an improvement slightly above 53% in execution time over the case of all inequality types removed from the program.

Observing table A9., in Appendix A, it can be noticed, however, that inequality type 4 showed a weak effect on the computation time for all the functions tested. Inequality type 5, instead, produced a greater effect on the execution time, but this effect appears to depend mainly on the particular function tested. For most of the functions, however, the tendency was to decrease execution time.

We can conclude then, that for the NOR design using the feed-forward formulation all inequalities, except the triangular condition (type 4) appear to have an effect in reducing execution time. Since inequality type 4 showed a weak effect most of the time, and in some instances a strongly

adverse effect we are tempted to conclude that this inequality type should be removed from the feed-forward formulation program but again further research, especially for designs with more than five gates, is desirable to establish firmer conclusions in this respect.

Table 10 shows the effect the different inequality types have on execution time for the feed-forward formulation.

case	most effective	marginally effective	adversely effective
5 gates removing inequalities	5,1	2,4,3	
6 gates removing inequalities	1,3,2	5,4	
5 gates adding inequalities	1,2,5,3	4	
6 gates adding * inequalities	1		4

* This was incompletely tested and only one function was used.

Table 10. Comparison of the effect of additional inequalities on the NOR design with feed-forward formulation for three variable functions.

In observing Tables 6 and 10 for the NOR design with the all-interconnection and the feed-forward formulations, respectively, it is observed that inequality types 2 and 3 are always effective in reducing execution time, inequality type 4 has weak or adverse influence, in general, for both formulations, and, in contrast, inequality types 2, and 5 which showed almost no effect and a slightly adverse effect, respectively, for the all-interconnection formulation become more effective in the case of the feed-forward formulation. Then, and as a general rule, for NOR designs with all-interconnection formulation inequality types 1 and 3 should always appear in the program, inequality type 2 may or may not be removed without affecting execution time while inequality types 4 and 5 should be removed in designs with five or six gates but should probably be included in designs with seven or more gates.

For the feed-forward formulation, instead, all inequality types should be included in the program but more attention should be given to the inclusion of inequality types 4 and 5 in designs with more than five gates since their influence appears to be determined to a great extent by the individual functions.

3.2 NOR-AND design with all-interconnection formulation

For this design case, results shown in table 11, which is a summary of tables A 15 and A 16, demonstrated that removal of additional inequalities from the program does not produce additive effects on

case	5 gates			6 gates		
	$\overline{t}$	$\overline{I}$	$\overline{FO}$	$\overline{t}$	$\overline{I}$	$\overline{FO}$
All inequalities included	8.4	171	46	45.62	847	195
All except type 6*	14.48	353	86	77.92	1530	270
All except type 2	8.05	171	46	44.55	847	195
All except type 3	10.02	202	52	57.80	1034	217
All except type 4	7.83	172	46	45.58	886	196
All except type 5	7.59	172	46	41.64	853	197
All except type 7 **	7.73	177	48	42.98	897	210
All except type 8 **	8.06	177	48	44.70	870	201
All except types 2,6	14.05	353	86	77.52	1530	270
All except types 3,6	15.74	383	97	90.40	1712	311
All except types 4,6	13.66	355	86	75.90	1604	271

Table 11. Three variable, NOR-AND design.
(All-interconnection formulation).
(Summary of Tables A 15. and A 16.)

(continued)

case	5 gates			6 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All except types 5,6	13.51	354	86	74.52	1550	272
All except types 7,6	13.76	357	87	76.60	1571	275
All except types 8,6	13.56	355	87	73.78	1550	271
All except types 2,3	10.80	202	52	58.8	1034	217
All except types 2,4	7.60	172	46	42.48	886	196
All except types 2,5	7.55	172	46	41.56	853	197
All except types 2,7	7.77	177	48	43.12	897	210
All except types 2,8	8.04	177	48	42.84	870	201
All except types 3,4	9.74	205	52	55.52	1085	219
All except types 3,5	9.63	203	52	56.68	1043	220
All except types 3,7	9.85	219	60	57.92	1152	250

(continued from previous page)

Table 11. Three variable, NOR-AND design.
(All-interconnection formulation).
(Summary of Tables A 15. and A 16.)

(continued)

case	5 gates			6 gates		
	$\bar{t}$	$\bar{I}$	$\overline{FO}$	$\bar{t}$	$\bar{I}$	$\overline{FO}$
All except types 3,8	9.76	210	54	54.82	1072	223
All except types 4,5	7.57	173	46	43.30	892	198
All except types 4,7	8.03	190	53	43.95	1000	221
All except types 4,8	7.66	178	48	42.22	909	202
All except types 5,7	7.50	177	48	41.54	903	212
All except types 5,8	7.58	179	48	40.96	882	204
All except types 7,8	7.50	183	51	41.58	934	221
Maximum of the Averages	15.74	383	97	90.40	1712	311
Minimum of the Averages	7.50	171	46	41.54	847	195
Number of Functions Tested	5			4		

(continued from the previous page)

* corresponds to type 1 in NOR design
** other triangular conditions

$\bar{t}$: average computation time in seconds.
$\bar{I}$: average of total number of Iterations for the solution.
$\overline{FO}$: average of number of iterations to obtain First Optimal solution.

Table 11. Three variable, NOR-AND design.
(All-interconnection formulation).
(Summary of Tables A 15. and A 16.)

the execution time, but the effect of removing inequality types in pairs reinforces the results of removing inequality types individually in the same sense as in the NOR case.

It can be observed in table 11 that inequalities type 6 and type 3 produced the largest execution times when individually removed from the program, and that inequality types 5, 7 and 8 reduce the execution times when removed individually.

Conclusions for this case follow the same tendency as in the NOR design case with all-interconnection formulation, i.e. additional inequalities which restrict in some way the number of inputs or outputs to the gates (inequalities type 6 and type 3), have the greatest effect in reducing execution time when included in the program to solve the optimal design problem. Also additional inequalities related to the triangular condition (inequality types 5 and 7) produce the effect of increasing execution time when included in the program. Then inequality type 6 and 3 should always be included in the program and inequality types 5 and 7 should be removed from the program without an adverse effect in execution time. As inequality types 2, 4, and 8 do not produce a significant effect on executions time, they may or may not be removed from the program, without affecting the execution time in a significant way.

3.3 NOR-NAND design with all-interconnection formulation

For the ten functions tested in the NOR-NAND design case we observe in table 12 (see table A 10 for details), that the largest figure for average computation time is given by inequality type 12 followed by those figures given by inequality types 3 and 4. Adverse effects

case	$\overline{t}$	$\overline{I}$	$\overline{FO}$
All inequalities included	7.38	168	62
All except type 9 *	7.15	168	62
All except type 2	7.26	168	62
All except type 3	10.00	228	88
All except type 4	7.96	183	76
All except type 5	7.20	169	66
All except type 10 **	7.12	168	62
All except type 11 **	6.86	168	62
All except type 12 ***	12.68	292	125
Maximum of the Averages	12.68	292	125
Minimum of the Averages	6.86	168	62
Number of Functions Tested	10		

* corresponds to type 1 of NOR design.
** other type of triangular condition.
*** unique for NOR-NAND design.

$\overline{t}$: average computation time in seconds.
$\overline{I}$: average of total number of iterations for the solution.
$\overline{FO}$: average of number of iterations to obtain First Optimal Solution.

Table 12. Three variable, five gate NOR-NAND design. (All-interconnection formulation). (Summary of table A 10.)

are produced by inequalities type 11, type 10 and type 9, while inequalities type 2 and type 5 have little effect on the computation time.

We can conclude that inequalities type 12, type 3 and type 4 should not be removed from the program while inequalities type 11, type 10 and type 9 should be removed from the program if speed-up in execution time is desired. The rest of the additional inequalities, inequality types 2 and 5 may be left in or taken out from the program without affecting the execution time.

3.4 AND-OR design with all-interconnection formulation

As it was shown in table 1 for this design case inequality types 3 and 15 were not tested and actually they were not included in the program at any time since storage requirements were too large to be justified at the moment the program was written and tested. In addition, the authors of the program thought that these two types of inequalities were not very effective in reducing execution time. In all tested cases inequalities type 3 and type 15 are removed from the program. It should be noticed, observing table 13, that what happened in the NOR design case with the all-interconnection formulation appears to be reversed in the present case since now the elimination of the additional inequality related to the triangular condition, inequality type 14, produces the largest figure in execution time. This inequality, in turn, is followed by the execution time figures produced when inequalities type 16 and type 13 are removed. Almost no effect is produced when inequalities type 17 and type 2 are removed from the program.

case	$\overline{t}$	$\overline{I}$	$\overline{FO}$
All inequalities included	37.90	589	57
All except type 13*	57.77	893	62
All except type 2	37.58	591	57
All except type 14**	85.80	1663	108
All except type 16***	61.89	1091	78
All except type 17***	38.02	589	57
Maximum of the Averages	85.80	1663	108
Minimum of the Averages	37.58	589	57
Number of Functions Tested	10		

* corresponds to type 1.
** another triangular condition.
*** unique for AND-OR design.

$\overline{t}$: average computation time in seconds.
$\overline{I}$: average of total number of iterations for the solution.
$\overline{FO}$: average of number of iterations to obtain First Optimal solution.

Table 13. Four variable, five AND-OR gate design.
(All-interconnection formulation)
(Summary of table A 11.)

All of this implies that inequality types 14, 16 and 13 should be included in the program in order to obtain the shortest execution times, and inequality types 2 and 17 may mor may not be removed from the program without significantly affecting the execution time for the design of five AND or OR gate networks with the all-interconnection formulation program.

Since, in this case, and the NOR-NAND case, only five gate functions were used, it is suggested that more research should be done using functions which are implemented with a larger number of gates to obtain enough information that would permit more general and fundamented conclusions.

Table 14. shows the effect of additional inequalities for the last three design cases discussed.

case	most effective	marginally effective	adversely effective
NOR-AND	6,3	2,4,8	5,7
NOR-NAND	12,3,4	2,5	11,10,9
AND-OR	14,16,13	17,2	

Table 14. Comparison of the effect of additional inequalities on NOR-AND, NOR-NAND, and AND-OR, designs with the all-interconnection formulation for three variable functions.

3.5 Overall Conclusion

Tables 6, 10 and 14 show the effects of additional inequalities on the execution time for the design cases of interest in this paper.

Observation of those tables lead us to conclude that in general: 1) The most effective types of inequalities in terms of reduction of execution time are:

a) those which are concerned with the number of connections and interconnections permitted to the gates, such as type 1 for NOR design and its corresponding types in other design cases: type 6 for NOR-AND design, type 13 for AND-OR (but notice the exception of type 9 for NOR_NAND design), and

b) those inequalities which prohibit certain types of output interconnections as inequality type 3 in the cases in which this type was tested. In this group can also be classified inequality type 12, applicable to the NOR-NAND design.

2) Inequalities which consistently show weak or almost negligible effect on the computation time are those corresponding to type 2 with the exception of the feed-forward formulation for NOR design;

3) The most adverse effect on execution time is presented by inequalities related to the triangular condition with the exceptions of some cases in the feed-forward formulation for NOR design and for the AND-OR design with the all-interconnection formulation.

These conclusions show only the apparent tendency of the effect of the inequality types on the computation time for different cases of logical design. In a specific case it is recommended to refer to tables 6, 10 or 14, whichever corresponds, and to the adjoining conclusions to establish in a more proper way which inequality types should be included, or which should be excluded from the programs to obtain improvement of execution time.

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APPENDIX A

TABLES OF DETAILED COMPUTATIONAL RESULTS

The following tables show the results for each function used in the different design cases. the tables include: an identification number for the function,taken from the literature as given below; execution time in seconds (t) , total number of iterations to exhaust all possible optimal networks (I), and the number of iterations until the first optimal solution is generated (FO) , for each of the computer runs made.

At the end of each table the averages for the three numerical values for each run are presented, but for the number of iterations (I and FO) we took the smallest integer greater or equal to the corresponding average.

The functions were taken from the literature as follows:

For NOR design,three variable case from [4],

For NOR-NAND design from [7],

For AND-OR design case and four variable NOR design case from [2 and 3]

For NOR-AND design from [1] ,and

For the one-bit full adder design case from [8] .

FUnctions numbered	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
after [4]	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
36	0.74	18	6	1.06	34	6	0.73	18	6	0.79	24	10	0.69	18	6	0.73	18	6
22	1.11	36	12	1.28	48	12	1.13	36	12	1.24	40	14	1.03	36	12	1.23	40	12
27	1.91	68	17	2.02	70	17	1.84	68	17	1.89	68	17	1.89	68	17	1.93	68	17
29	0.66	14	12	0.71	14	12	0.68	14	12	0.76	22	14	0.59	14	12	0.59	14	12
30	1.03	32	15	1.16	33	15	1.08	32	15	1.13	37	18	0.96	32	15	1.01	32	15
31	1.04	36	16	1.29	43	16	1.04	36	16	1.14	37	17	1.03	36	16	0.99	36	16
28	0.61	14	11	0.68	14	11	0.59	14	11	0.64	18	13	0.56	14	11	0.61	14	11
33	0.96	32	9	1.43	50	9	1.11	32	9	0.99	32	9	0.89	32	9	0.94	32	9
50	1.06	33	9	1.21	33	9	1.06	33	9	1.18	37	9	1.04	33	9	0.96	33	9
40	1.09	30	19	1.51	44	33	1.04	30	19	1.14	34	22	0.99	30	19	1.03	30	19
47	0.88	26	17	1.39	48	39	0.89	26	17	0.89	26	17	0.81	26	17	0.88	26	17
48	0.66	18	7	0.71	20	7	0.73	18	7	0.83	18	7	0.63	18	7	0.69	18	7

Table A1. Three variable, five NOR gate design. (All-interconnection formulation).

(continued)

Functions numbered after [4]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
34	0.83	26	7	1.46	46	7	0.88	26	7	0.74	26	7	0.81	26	7	0.79	26	7
44	0.73	20	10	0.69	20	10	0.73	20	10	0.78	24	10	0.69	20	10	0.74	20	10
35	0.93	30	8	1.66	64	8	0.93	30	8	1.11	30	8	0.89	30	8	1.09	36	8
12D	0.89	28	8	1.09	40	8	0.88	28	8	0.91	28	8	0.81	28	8	0.83	28	8
51	0.73	24	11	0.73	24	11	0.78	24	11	0.73	28	11	0.68	24	11	0.73	24	11
37	0.89	22	8	1.19	40	8	0.79	22	8	0.88	22	8	0.83	22	8	0.81	22	8
26	1.28	28	8	1.24	33	8	1.21	28	8	1.16	28	8	1.27	28	8	1.14	28	8
42	1.09	30	25	1.39	50	35	1.06	30	25	1.58	48	41	1.03	30	25	1.03	30	25
49	0.86	23	8	0.88	23	8	0.88	23	8	0.98	27	8	0.91	23	8	0.86	23	8
39	1.48	41	19	1.76	51	19	1.68	41	19	1.69	55	28	1.51	41	19	1.44	41	19
averages	0.97	29	12	1.20	39	14	0.98	29	12	1.05	33	14	0.93	29	12	0.96	30	13

(continued from previous page)

Table A1. Three variable, five NOR gate design. (All-interconnection formulation).

Functions numbered after[4]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
58	7.33	253	30	7.38	261	30	7.22	253	30	8.65	293	30	7.60	297	30	7.08	253	30
59	5.32	160	20	7.37	170	20	5.35	160	20	7.55	258	29	4.92	168	20	5.02	160	20
61	5.70	173	9	5.99	189	10	5.65	173	9	7.18	215	12	5.44	185	9	5.40	173	9
55	4.50	143	32	6.15	199	32	4.37	143	32	5.80	197	41	4.24	157	32	4.32	143	32
60	7.73	218	35	8.17	260	38	7.27	218	35	8.65	268	38	7.40	262	35	7.20	218	35
64	2.44	57	17	2.47	63	17	2.31	57	17	2.46	67	17	2.06	57	17	2.14	57	17
54	3.59	103	26	3.69	111	26	3.42	103	26	3.56	107	26	3.31	107	26	3.29	103	26
68	6.98	202	117	9.35	284	195	6.87	202	117	8.75	276	183	8.13	282	151	6.82	202	117
56	7.10	222	52	8.55	268	83	7.10	222	52	8.25	262	67	7.13	248	52	6.90	222	52

Table A2. Three variable, six NOR gate design. (All-interconnection formulation.)
(continued)

Functions numbered after[4]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
69	5.77	158	74	6.53	190	98	5.40	158	74	6.80	220	104	5.25	172	74	5.00	178	74
53	3.09	85	11	3.24	95	11	2.85	85	11	2.91	89	11	2.75	85	11	2.71	85	11
57	6.93	216	11	6.97	241	11	6.48	216	11	7.82	259	11	6.87	254	11	6.32	216	11
67	2.77	63	11	3.07	77	11	2.75	63	11	2.96	71	11	2.64	63	11	2.82	63	11
66	6.25	184	11	6.47	208	11	5.98	184	11	7.22	236	11	6.80	226	11	5.76	184	11
63	4.02	109	22	4.11	117	22	3.79	109	22	5.09	157	28	3.54	109	22	3.61	109	22
averages	5.30	157	32	5.96	182	41	5.12	157	32	6.24	199	42	5.20	179	35	4.96	158	32

(continued from the previous page

Table A2. Three variable, six NOR gate design. (All-interconnection formulation.)

Functions numbered after [4]		76	72	77	73	80	79	averages
All	t	19.56	42.38	34.24	36.35	40.51	24.46	32.92
inequalities	I	473	1 065	869	953	983	582	821
included	FO	274	17	182	51	33	38	100
All	t	19.43	46.64	39.02	37.34	46.16	24.57	35.52
except	I	495	1215	1015	1017	1167	608	920
type 1	FO	288	17	202	55	33	38	106
All	t	19.00	42.18	34.14	35.04	39.33	23.14	32.14
except	I	473	1065	869	953	983	582	821
type 2	FO	274	17	182	51	33	38	100
All	t	25.48	52.58	38.30	40.20	50.96	27.77	39.22
except	I	668	1400	1042	1100	1388	712	1052
type 3	FO	421	23	208	53	37	43	131
All	t	17.73	42.36	36.19	38.30	46.82	25.77	34.52
except	I	501	1235	1087	1237	1345	754	1027
type 4	FO	274	17	182	51	33	38	100
All	t	17.92	40.80	33.13	33.01	38.15	22.57	30.93
except	I	473	1065	869	953	983	582	821
type 5	FO	274	17	182	51	33	38	100

Table A3. Three variable, seven NOR gate design. (All-interconnection formulation).

Functions numbered after [3]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
28AF	2.06	38	21	2.91	60	43	2.11	38	21	2.59	50	27	2.06	38	21	2.12	38	21
2AEA	2.03	42	11	2.94	66	11	2.17	42	11	2.44	44	12	1.89	42	11	1.89	42	11
2CCC	2.66	54	8	2.76	58	8	2.84	54	8	3.07	56	9	2.66	54	8	2.69	54	8
6AAA	3.04	64	32	3.11	68	36	3.06	64	32	3.47	64	32	2.96	64	32	3.06	64	32
8183	2.39	38	17	2.41	38	17	2.59	38	17	2.66	48	19	2.32	38	17	2.54	38	17
889F	1.46	25	9	1.49	25	9	1.56	25	9	1.93	35	10	1.41	25	9	1.51	25	9
008B	1.96	36	7	2.10	42	7	2.36	36	7	2.37	46	12	1.88	36	7	1.93	36	7
00EF	1.93	34	6	2.29	46	6	2.22	34	6	2.27	50	9	1.94	34	6	2.29	34	6
01AF	2.19	40	10	3.31	68	10	2.36	40	10	2.92	66	18	2.06	40	10	2.31	40	10
08BF	2.56	44	9	3.26	62	9	2.66	44	9	3.05	62	12	2.56	44	9	2.41	44	9
averages	2.22	42	13	2.66	54	16	2.39	42	13	2.68	53	16	2.17	42	13	2.28	42	13

Table A4. Four variable, five NOR gate design. (all-interconnection formulation).

Functions numbered after [3]		011F	0255	0BD1	0FF1	6BFF	averages
All	t	37.04	37.98	20.10	22.13	39.38	31.32
inequalities	I	658	757	385	454	926	636
included	FO	13	136	14	12	34	42
All	t	56.32	53.23	22.09	25.09	42.68	39.88
except	I	1014	1077	447	520	1008	814
type 1	FO	13	136	14	12	34	42
All	t	40.35	40.68	20.43	23.07	40.23	32.95
except	I	658	757	385	454	926	636
type 2	FO	13	136	14	12	34	42
All	t	64.48	57.15	22.46	25.00	53.43	44.50
except	I	1412	1181	453	528	1282	972
type 3	FO	15	318	18	12	38	81
All	t	40.01	40.81	20.81	24.96	44.24	34.16
except	I	718	881	433	540	1094	734
type 4	FO	13	136	14	12	34	42
All	t	37.05	36.02	17.85	20.93	36.47	29.66
except	I	658	757	385	454	926	636
type 5	FO	13	136	14	12	34	42

Table A5. Four variable, six NOR gate design. (All-interconnection (formulation).

Function numbered after [3]		8228
All inequalities included	t	117.17
	I	2071
	FO	448
All except type 1	t	119.42
	I	2091
	FO	456
All except type 2	t	119.49
	I	2071
	FO	448
All except type 3	t	159.38
	I	2932
	FO	684
All except type 4	t	133.16
	I	2587
	FO	448
All except type 5	t	120.70
	I	2327
	FO	488

Table A6. Four variable, seven NOR gate design. (All-interconnection formulation).

Functions numbered after[4]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
37	3.78	91	14	4.75	131	18	3.63	91	15	4.15	103	18	4.08	107	16	5.85	147	23
26	3.73	133	61	5.83	207	167	3.97	131	67	3.61	133	61	4.68	157	43	2.68	71	41
42	3.98	89	11	4.26	119	12	3.60	83	11	3.82	97	13	3.82	97	10	4.13	93	15
49	3.80	93	7	5.16	167	7	3.03	71	6	3.50	97	7	3.63	93	7	2.78	61	5
39	5.11	109	10	5.76	143	11	5.65	133	10	5.38	119	11	5.51	117	9	6.93	197	11
32	4.71	121	21	6.26	195	29	5.18	157	28	5.46	147	38	5.03	139	25	10.59	319	65
27	4.66	127	66	5.40	175	128	4.46	133	70	4.28	129	68	4.96	167	40	4.68	145	39
36	3.73	89	14	4.80	127	18	3.23	87	15	4.08	103	20	3.87	107	16	5.10	131	27
29	4.00	103	82	4.66	137	118	3.73	93	74	4.18	109	88	4.45	131	106	4.18	115	54
30	3.67	93	16	4.73	133	20	3.30	91	17	4.05	107	23	3.60	105	18	4.35	95	23
31	3.75	101	16	4.78	135	20	3.30	95	17	3.92	115	22	3.80	111	18	4.28	111	23
28	4.23	111	86	5.61	203	176	3.80	97	78	4.33	113	88	4.78	157	128	4.15	111	48

Table A7. Three variable, five NOR gate design. (Feed-forward formulation).

Functions numbered after[4]	All inequalities included			All except type 1			All except type 2			All except type 3			All except type 4			All except type 5		
	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
33	3.80	101	16	4.53	137	20	3.35	99	17	3.90	113	20	3.73	115	18	4.75	119	25
50	3.95	121	12	5.40	195	16	3.27	95	11	3.87	127	12	3.65	117	12	2.97	89	10
40	6.21	125	112	5.60	131	116	6.38	147	119	6.53	149	136	6.00	131	127	8.52	281	70
47	3.28	99	56	3.87	131	71	3.45	107	72	3.22	107	64	3.37	107	50	4.28	137	15
48	3.82	119	40	5.30	215	57	3.98	131	52	3.71	119	40	4.48	139	37	3.10	81	8
34	5.30	181	28	5.40	211	35	7.09	253	46	6.33	221	40	5.95	207	31	10.82	343	135
44	4.53	133	44	4.95	171	39	5.13	149	19	4.61	143	48	4.96	145	21	6.18	169	49
35	5.90	213	28	7.44	311	35	11.97	463	44	6.73	243	36	7.58	287	31	16.91	619	221
12D	3.72	115	16	4.63	139	20	3.28	95	17	4.50	139	25	3.97	121	18	4.41	113	45
51	3.98	127	12	4.41	147	12	6.10	201	12	4.33	137	12	4.63	151	13	6.06	207	11
averages	4.26	118	35	5.16	168	53	4.58	137	38	4.48	131	41	4.56	137	37	5.80	171	44

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Table A7. Three variable, five NOR gate design. (Feed-forwaed formulation).

Functions numbered after[4]		58	59	61	55	60	averages
All	t	63.17	66.60	63.23	63.12	54.67	62.16
inequalities	I	1847	1783	1951	1823	1661	1813
included	FO	99	162	152	208	162	157
All	t	99.16	113.91	165.84	122.43	109.70	122.20
except	I	3285	3671	6403	4261	3749	4274
type 1	FO	199	265	351	446	304	293
All	t	76.80	75.48	77.45	91.31	66.10	77.42
except	I	2269	1939	2101	2569	1911	2158
type 2	FO	105	168	265	241	172	191
All	t	71.44	84.95	95.95	70.86	71.62	78.96
except	I	2121	2425	3017	2141	2281	2397
type 3	FO	126	339	230	267	339	261
All	t	74.80	72.34	69.53	69.36	64.34	70.07
except	I	2247	1937	2055	1885	1907	2007
type 4	FO	61	196	170	472	210	222
All	t	97.25	83.42	64.55	43.15	76.83	73.04
except	I	2777	2267	1517	1205	2193	1992
type 5	FO	43	46	44	51	160	69

Table A8. Three variable ,six NOR gate design. (Feed-forward formulation).

Functions numbered after[4]		48	43	47	40	28
All inequalities removed	t	14.33	10.42	14.32	25.90	13.40
	I	479	349	499	1015	441
	FO	12	14	21	165	158
With type 1 only	t	4.31	5.41	6.93	17.99	4.85
	I	123	155	249	735	137
	FO	12	14	17	159	62
With type 2 only	t	10.24	8.32	10.90	21.19	9.99
	I	345	269	389	875	321
	FO	12	14	21	114	134
With type 3 only	t	14.02	10.65	14.37	21.89	13.20
	I	475	345	493	779	441
	FO	8	10	19	87	158
With type 4 only	t	13.92	11.57	14.15	29.03	12.75
	I	473	341	477	1151	411
	FO	8	10	19	217	150
With type 5 only	t	16.41	10.95	7.11	11.00	15.31
	I	669	403	265	327	555
	FO	176	43	93	279	349

Table A9. Three variable five NOR gate design.
(Feed-forward formulation).
(Adding inequalities one-by-one).

(continued)

Functions numbered after[4]		29	27	39	42	37	averages
All	t	10.06	10.31	17.74	11.05	14.90	14.24
inequalities	I	317	345	609	339	491	489
removed	FO	125	95	11	24	45	67
With	t	5.18	5.28	10.24	5.85	8.39	7.44
type 1	I	151	169	151	161	255	249
only	FO	76	45	11	19	33	49
With	t	8.14	8.19	14.30	9.01	12.50	11.28
type 2	I	261	273	497	275	413	397
only	FO	117	87	11	24	45	58
With	t	9.57	10.22	17.03	10.97	15.01	13.69
type 3	I	309	341	569	333	483	457
only	FO	119	95	10	20	39	113
With	t	9.69	10.37	18.29	11.74	14.70	14.62
type 4	I	297	319	561	333	469	484
only	FO	115	96	11	20	37	69
With	t	11.67	17.14	8.99	8.61	8.91	11.61
type 5	I	399	555	291	249	269	399
only	FO	227	286	17	35	35	154

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Table A9. Three variable, five NOR gate design.
(Feed-forward formulation).
(Adding inequalities one-by-one).

Functions numbered	All inequalities included			All except type 9			All except type 2			All except type 3			All except type 4			All except type 5		
after [7]	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO	t	I	FO
26	12.95	341	23	12.87	341	23	12.87	341	23	16.08	417	23	13.57	359	23	12.48	343	23
32	6.18	134	90	6.00	134	90	6.06	134	90	8.84	199	147	6.93	158	114	5.95	134	90
30	6.53	139	53	6.36	139	53	6.46	139	53	8.81	195	67	6.74	139	53	6.43	139	53
31	6.99	156	37	6.91	156	37	7.33	156	37	9.40	207	43	8.03	182	59	6.76	156	37
27	6.93	135	15	6.78	135	15	6.89	135	15	9.06	191	17	7.39	135	15	6.74	135	15
40	6.78	142	109	6.34	142	109	6.44	142	109	8.77	189	147	7.46	166	133	6.46	144	111
28	5.10	91	35	4.81	91	35	4.88	91	35	6.64	141	48	5.16	91	35	5.08	91	35
34	7.48	160	141	7.04	160	141	7.23	160	141	10.65	235	210	8.23	186	167	7.16	162	143
38	7.96	209	60	7.68	209	60	7.81	209	60	11.90	290	83	8.56	229	80	8.06	211	60
42	6.94	164	56	6.74	164	56	6.66	164	56	9.82	215	88	7.54	184	76	6.96	170	56
averages	7.38	168	62	7.15	168	62	7.26	168	62	10.00	228	88	7.96	183	76	7.20	169	66

Table A10. Three variable, five NOR-NAND gate design.
(All-interconnection formulation).
(continued)

Functions numbered	All except type 10			All except type 11			All except type 12		
after 7	t	I	FO	t	I	FO	t	I	FO
26	13.02	341	23	12.70	341	23	21.15	541	25
32	6.10	134	90	6.16	134	90	11.55	269	213
30	6.49	139	53	6.26	139	53	11.74	245	101
31	6.89	156	37	6.51	156	37	12.47	285	101
27	6.54	135	15	6.44	135	15	12.50	259	35
40	6.16	142	109	5.91	142	109	11.24	245	196
28	4.73	91	35	4.51	91	35	8.77	173	67
34	6.99	160	141	6.58	160	141	13.38	303	276
38	7.64	209	60	7.24	209	60	12.48	321	112
42	6.61	164	56	6.29	164	56	11.55	273	124
averages	7.12	158	62	6.86	168	62	12.68	292	125

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Table A10. Three variable, five NOR-NAND gate design.
(All-interconnection formulation).

Functions numbered after 2		42	41	40	39	38
All inequalities included	t	37.40	34.73	36.78	35.11	31.16
	I	583	573	573	519	507
	FO	49	36	24	15	12
All except type 13	t	56.83	55.57	51.76	52.67	47.41
	I	843	879	793	807	733
	FO	49	36	24	15	12
All except type 2	t	37.51	36.06	35.38	32.55	32.69
	I	583	573	573	519	507
	FO	49	36	24	15	12
All except type 14	t	86.15	79.78	84.22	74.10	75.43
	I	1671	1569	1619	1459	1453
	FO	71	40	32	17	14
All except type 16	t	60.61	57.61	61.36	58.20	56.58
	I	1091	1065	1075	1007	1019
	FO	57	38	28	17	14
All except type 17	t	38.04	36.25	36.56	33.80	32.67
	I	583	573	573	519	507
	FO	49	36	24	15	12

Table A11. Four variable, five AND-OR gate design. (All-interconnection formulation).

(continued)

Functions numbered after 2		36	29	24	23	17	averages
All inequalities included	t	37.93	39.99	57.13	41.75	26.98	37.90
	I	591	627	891	629	395	589
	FO	40	80	89	8	216	57
All except type 13	t	58.64	60.74	94.99	69.96	29.17	57.77
	I	917	947	1463	1099	441	893
	FO	40	82	91	8	262	62
All except type 2	t	38.84	38.68	56.40	39.28	28.39	37.58
	I	591	627	897	635	399	591
	FO	40	80	89	8	216	57
All except type 14	t	82.82	88.56	131.29	99.18	56.50	85.80
	I	1611	1771	2605	1935	935	1663
	FO	56	180	153	10	507	108
All except type 16	t	61.97	62.21	83.52	64.93	51.94	61.89
	I	1071	1113	1479	1087	895	1091
	FO	46	98	97	10	371	78
All except type 17	t	37.33	38.96	59.14	40.31	27.19	38.02
	I	591	627	891	629	395	589
	FO	40	80	89	8	216	57

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Table All. Four variable, five AND-OR gate design. (All-interconnection formulation).

Functions numbered after [4]		37	26	42	49	39	averages
All inequalities included	t	0.89	1.28	1.09	0.86	1.48	1.12
	I	22	28	30	23	41	29
	FO	8	8	25	8	19	14
All except type 1	t	1.19	1.24	1.39	0.88	1.76	1.29
	I	40	33	50	23	51	40
	FO	8	8	35	8	19	16
All except type 2	t	0.79	1.21	1.06	0.88	1.68	1.12
	I	22	28	30	23	41	29
	FO	8	8	25	8	19	14
All except type 3	t	0.88	1.16	1.58	0.98	1.69	1.[illegible]
	I	22	28	48	27	55	3[illegible]
	FO	8	8	41	8	28	19
All except type 4	t	0.83	1.27	1.03	0.91	1.51	1.11
	I	22	28	30	23	41	29
	FO	8	8	25	8	19	14
All except type 5	t	0.81	1.14	1.03	0.86	1.44	1.06
	I	22	28	30	23	41	29
	FO	8	8	25	8	19	14

Table A12. Three variable, five NOR gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after[4]		37	26	42	49	39	averages
All	t	1.29	1.38	1.46	1.03	1.79	1.39
except	I	40	33	50	23	51	40
types 1,2	FO	8	8	35	8	19	16
All	t	1.36	1.31	1.98	1.06	2.01	1.54
except	I	40	33	62	31	69	47
types 1,3	FO	8	8	41	8	28	19
All	t	1.11	1.19	1.31	0.88	1.63	1.22
except	I	40	33	50	23	51	40
types 1,4	FO	8	8	35	8	19	16
All	t	1.09	1.18	1.31	0.88	1.66	1.22
except	I	40	33	50	23	51	40
types 1,5	FO	8	8	35	8	19	16
All	t	0.86	1.19	1.63	0.96	1.73	1.27
except	I	22	28	48	27	55	36
types 2,3	FO	8	8	41	8	28	19
All	t	0.87	1.19	1.11	0.88	1.49	1.10
except	I	22	28	30	23	41	29
types 2,4	FO	8	8	25	8	19	14

(continued from the previous page)

Table A12. Three variable, five NOR gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [4]		37	26	42	49	39	averages
All	t	0.82	1.18	1.01	0.84	1.53	1.08
except	I	22	28	30	23	41	29
types 2,5	FO	8	8	25	8	19	14
All	t	0.78	1.16	1.54	0.96	1.56	1.20
except	I	22	28	50	29	55	37
types 3,4	FO	8	8	41	8	28	19
All	t	0.83	1.11	1.59	0.88	1.71	1.22
except	I	22	28	48	27	57	37
types 3,5	FO	8	8	41	8	28	19
All	t	0.78	1.04	0.94	0.81	1.33	0.98
except	I	22	28	30	23	41	29
types 4,5	FO	8	8	25	8	19	14

(continued from previous page)

Table A12. Three variable, five NOR gate design.
(All-interconnection formulation.)

Functions numbered after [4]		53	57	67	66	63	averages
All	t	3.09	6.93	2.77	6.25	4.02	4.61
inequalities	I	85	216	63	184	109	132
included	FO	11	11	11	11	22	14
All	t	3.24	6.97	3.07	6.47	4.11	4.77
except	I	95	241	77	208	117	128
type 1	FO	11	11	11	11	22	14
All	t	2.85	6.48	2.75	5.98	3.79	4.37
except	I	85	216	63	184	109	132
type 2	FO	11	11	11	11	22	14
All	t	2.91	7.82	2.96	7.22	5.09	5.20
except	I	89	259	71	236	157	163
type 3	FO	11	11	11	11	28	15
All	t	2.75	6.87	2.64	6.80	3.54	4.52
except	I	85	254	63	226	109	148
type 4	FO	11	11	11	11	22	14
All	t	2.71	6.32	2.82	5.76	3.61	4.24
except	I	85	216	63	184	109	132
type 5	FO	11	11	11	11	22	14

Table A13. Three variable, six NOR-gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [4]		53	57	67	66	63	averages
All except types 1,2	t	3.29	7.00	3.04	6.33	4.11	4.75
	I	95	241	77	208	117	128
	FO	11	11	11	11	22	14
All except types 1,3	t	3.40	8.00	3.42	7.27	5.04	5.42
	I	97	273	85	238	165	172
	FO	11	11	11	11	28	15
All except types 1,4	t	3.42	6.90	2.76	6.67	3.76	4.70
	I	117	279	77	250	123	170
	FO	11	11	11	11	22	14
All except types 1,5	t	3.02	6.38	2.89	5.99	3.77	4.41
	I	95	241	77	208	117	128
	FO	11	11	11	11	22	14
All except types 2,3	t	2.94	7.72	2.91	7.27	4.80	5.12
	I	89	259	71	236	157	163
	FO	11	11	11	11	28	15
All except types 2,4	t	2.74	6.52	2.48	6.38	3.49	4.32
	I	85	254	63	226	109	148
	FO	11	11	11	11	22	14

(continued from the previous page)

Table A13. Three variable six NOR gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after[4]		53	57	67	66	63	averages
All	t	2.89	6.14	2.64	5.76	3.69	4.22
except	I	85	216	63	184	109	132
types 2,5	FO	11	11	11	11	22	14
All	t	2.86	7.50	2.84	7.67	4.64	5.10
except	I	91	299	79	278	157	181
types 3,4	FO	11	11	11	11	28	15
All	t	2.76	7.05	2.84	6.95	5.05	4.93
except	I	89	259	71	236	159	163
types 3,5	FO	11	11	11	11	28	15
All	t	2.64	5.80	2.34	5.84	3.24	3.97
except	I	85	254	63	226	109	148
types 4,5	FO	11	11	11	11	22	14

(continued from the previous page)

Table A13. Three variable, six NOR gate design.

Functions numbered after [4]		76	72	77	73	80	averages
All inequalities included	t	19.56	42.38	34.24	36.35	40.51	34.60
	I	473	1065	869	953	983	869
	FO	274	17	182	51	33	122
All except t pe 1	t	19.43	46.64	39.02	37.34	46.16	37.72
	I	495	1215	1015	1017	1167	982
	FO	288	17	202	55	33	119
All except type 2	t	19.00	42.18	34.14	35.04	39.33	33.94
	I	473	1065	869	953	983	869
	FO	274	17	182	51	33	122
All except type 3	t	25.48	52.58	38.30	40.20	50.96	41.50
	I	668	1400	1042	1100	1388	1120
	FO	421	23	208	53	37	149
All except type 4	t	17.73	42.36	36.19	38.30	46.82	36.28
	I	501	1235	1087	1237	1345	1081
	FO	274	17	182	51	33	122
All except type 5	t	17.92	40.80	33.13	33.01	38.15	32.60
	I	473	1065	869	953	983	869
	FO	274	17	182	51	33	122

Table A14. Three variable, seven NOR gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [4]		76	72	77	73	80	averages
All	t	19.36	46.70	39.09	37.19	46.12	37.69
except	I	4.95	1215	1015	1017	1167	982
types 1,2	FO	288	17	202	55	33	119
All	t	25.44	58.45	40.06	40.08	58.20	44.44
except	I	678	1526	1092	1120	1600	1204
types 1,3	FO	427	23	216	57	37	152
All	t	17.45	45.76	39.91	39.38	53.66	39.23
except	I	523	1399	1239	1301	1605	1214
types 1,4	FO	288	17	202	55	33	119
All	t	17.72	43.69	36.24	33.94	41.86	34.69
except	I	495	1215	1015	1017	1167	982
types 1,5	FO	288	17	202	55	33	119
All	t	25.36	52.03	38.02	39.76	49.88	41.01
except	I	668	1400	1042	1100	1388	1120
types 2,3	FO	421	23	208	53	37	149
All	t	17.93	42.79	36.15	38.05	46.46	36.28
except	I	501	1235	1087	1237	1345	1081
types 2,4	FO	274	17	182	51	33	122

(continued from the previous page)

Table A14. Three variable, seven NOR gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [4]		76	72	77	73	80	averages
All	t	18.08	40.10	32.43	34.17	37.97	32.55
except	I	473	1065	869	953	983	869
types 2,5	FO	274	17	182	51	33	122
All	t	22.88	50.08	39.00	41.63	55.81	41.88
except	I	718	1608	1286	1418	1836	1376
types 3,4	FO	425	23	208	53	37	150
All	t	24.64	49;87	34.92	36.95	46.07	38.49
except	I	678	1400	1042	1102	1388	1122
types 3,5	FO	421	33	208	53	37	149
All	t	15.55	37.88	32.09	33.91	41.81	32.24
except	I	501	1235	1087	1237	1345	1081
types 4,5	FO	274	17	18	51	33	122

(continued from the previous page)

Table A14. Three variable, seven NOR gate design.

Functions numbered after [1]		68	70	79	80	73	averages
All inequalities included	t	5.77	7.77	4.82	13.07	10.58	8.40
	I	121	155	93	261	225	171
	FO	24	39	11	54	101	46
All except type 6	t	13.22	16.87	7.10	21.51	13.72	14.48
	I	291	423	149	587	315	353
	FO	48	83	13	112	173	86
All except type 2	t	6.00	7.77	4.61	11.38	10.51	8.05
	I	121	155	93	261	225	171
	FO	24	39	11	54	101	46
All except type 3	t	7.53	9.53	5.32	14.49	13.26	10.02
	I	143	183	107	313	263	202
	FO	24	39	11	58	126	52
All except type 4	t	5.60	7.48	4.49	11.38	10.20	7.83
	I	121	155	93	261	229	172
	FO	24	39	11	54	101	46
All except type 5	t	5.44	7.28	4.32	11.03	9.88	7.59
	I	121	155	93	263	225	172
	FO	24	39	11	54	101	46

Table A15. Three variable, five NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		68	70	79	80	73	averages
All	t	5.65	7.38	4.30	11.16	10.16	7.73
except	I	125	163	93	273	227	177
type 7	FO	26	43	11	58	101	48
All	t	5.72	7.65	4.50	11.58	10.83	8.06
except	I	131	163	95	269	225	177
type 8	FO	26	39	11	60	101	48
All	t	12.46	16.47	7.00	20.99	13.34	14.05
except	I	291	423	149	587	315	353
types 2,6	FO	48	83	13	112	173	86
All	t	13.30	18.02	7.72	23.69	15.95	15.74
except	I	305	445	161	625	381	393
types 3,6	FO	48	87	13	120	214	97
All	t	11.98	15.77	6.75	20.60	13.19	13.66
except	I	291	4.23	153	587	319	355
types 4,6	FO	48	83	13	112	173	86
All	t	11.71	15.67	6.70	20.53	12.94	13.51
except	I	291	423	149	589	315	354
types 5,6	FO	48	83	13	112	173	86

(continued from the previous page)

Table A15. Three variable, five NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		68	70	79	80	73	averages
All	t	11.73	16.04	6.92	20.76	13.39	13.76
except	I	293	429	149	591	319	357
types 6,7	FO	48	87	13	112	173	87
All	t	11.86	15.77	6.95	20.25	13.01	13.56
except	I	295	423	149	591	315	355
types 6,8	FO	48	83	13	114	173	87
All	t	8.22	10.54	6.20	15.92	13.14	10.80
except	I	143	183	107	313	263	202
types 2,3	FO	24	39	11	58	126	52
All	t	5.45	7.37	4.32	10.89	9.95	7.60
except	I	121	155	93	261	229	172
types 2,4	FO	24	39	11	54	101	46
All	t	5.47	7.27	4.34	10.78	9.90	7.55
except	I	121	155	93	263	225	172
types 2,5	FO	24	39	11	54	101	46
All	t	5.49	7.33	4.40	10.94	10.69	7.77
except	I	125	163	93	273	227	177
types 2,7	FO	26	43	11	58	101	48

(continued from the previous page)

Table A15. Three variable.five NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		68	70	79	80	73	averages
All	t	5.97	7.82	4.67	11.63	10.13	8.04
except	I	131	163	95	269	225	177
types 2,8	FO	26	39	11	60	101	48
All	t	7.87	9.25	5.09	14.29	12.23	9.74
except	I	143	183	109	313	275	205
types 3,4	FO	24	39	12	58	127	52
All	t	7.27	9.43	5.10	13.85	12.51	9.63
except	I	143	183	107	315	263	203
types 3,5	FO	24	39	11	58	126	52
All	t	7.65	10.05	5.30	14.27	11.98	9.85
except	I	155	213	113	341	269	219
types 3,7	FO	28	59	13	70	128	60
All	t	8.15	9.71	5.15	13.89	11.93	9.76
except	I	155	191	111	327	265	210
types 3,8	FO	26	39	11	66	126	54
All	t	5.47	7.52	4.20	10.78	9.88	7.57
except	I	121	155	93	263	229	173
types 4,5	FO	24	39	11	54	101	46

(continued from the previous page)

Table A15. Three variable, five NOR-AND gate design.
(All-interconnection formulation)
(continued)

Functions numbered after [1]		68	70	79	80	73	averages
All except types 4,7	t	6.02	7.55	4.84	11.53	10.21	8.03
	I	135	173	105	283	253	190
	FO	32	49	11	64	107	53
All except types 4,8	t	5.99	7.43	4.24	10.91	9.71	7.66
	I	131	163	95	269	229	178
	FO	26	39	11	60	101	48
All except types 5,7	t	5.37	7.13	4.30	10.83	9.90	7.50
	I	125	163	93	275	227	177
	FO	26	43	11	58	101	48
All except types 5,8	t	5.50	7.22	4.32	10.93	9.91	7.58
	I	131	163	97	271	229	179
	FO	26	39	11	60	101	48
All except types 7,8	t	5.57	7.20	4.14	10.71	9.88	7.50
	I	135	171	99	281	229	183
	FO	28	43	13	64	103	51

(continued from the previous page)

Table A15. Three variable, five NOR-AND gate design.
(All-interconnection formulation.)

Functions numbered after[1]		101	100	105	99	averages
All inequalities included	t	29.28	61.63	45.39	46.19	45.62
	I	517	1189	827	855	847
	FO	26	520	193	41	195
All except type 6	t	49.13	108.70	82.20	71.66	77.92
	I	947	2123	1589	1461	1530
	FO	28	740	267	43	270
All except type 2	t	28.17	60.08	43.24	46.72	44.55
	I	517	1189	827	855	847
	FO	26	520	193	41	195
All except type 3	t	35.84	79.97	56.65	58.72	57.80
	I	615	1513	999	1009	1034
	FO	26	604	195	43	217
All except type 4	t	28.50	63.75	45.62	44.44	45.58
	I	517	1241	921	863	886
	FO	26	520	193	44	196
All except type 5	t	26.49	56.34	40.80	42.93	41.64
	I	517	1199	841	855	853
	FO	26	524	197	41	197

Table A16. Three variable, six NOR-AND gate design.
(All-interconnection formulation)
(continued)

Functions numbered after [1]		101	100	105	99	averages
All	t	26.94	59.18	42.11	43.72	42.98
except	I	543	1279	863	903	897
type 7	FO	26	578	195	41	210
All	t	28.92	60.12	43.14	46.65	44.70
except	I	523	1215	837	905	870
type 8	FO	26	538	195	43	201
All	t	47.67	106.09	83.59	72.71	77.52
except	I	947	2123	1589	1461	1530
types 2,6	FO	28	740	267	43	270
All	t	56.45	129.05	94.26	81.86	90.40
except	I	1059	2475	1749	1563	1712
types 3,6	FO	30	884	285	43	311
All	t	46.24	106.61	82.21	68.55	75.90
except	I	951	2233	1747	1483	1604
types 4,6	FO	28	742	267	46	271
All	t	45.74	102.14	79.60	70.60	74.52
except	I	947	2149	1643	1461	1550
types 5,6	FO	28	744	271	43	272

(continued from the previous page)

Table A16. Three variable, six NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		101	100	105	99	averages
All except types 6,7	t	46.26	107.19	81.63	71.35	76.60
	I	973	2179	1617	1513	1571
	FO	28	760	269	43	275
All except types 6,8	t	46.04	103.78	78.25	67.05	73.78
	I	951	2159	1593	1495	1550
	FO	10	762	267	45	271
All except types 2,3	t	37.98	84.69	55.91	56.64	58.80
	I	615	1513	999	1009	1034
	FO	26	604	195	43	217
All except types 2,4	t	26.22	57.25	43.59	42.84	42.48
	I	517	1241	921	863	886
	FO	26	520	193	44	196
All except types 2,5	t	26.02	56.17	41.05	43.03	41.56
	I	517	1199	841	855	853
	FO	26	524	197	41	197
All except types 2,7	t	26.97	60.02	41.73	43.76	43.12
	I	543	1279	863	903	897
	FO	26	578	195	41	210

(continued from the previous page)

Table A16. Three variable, six NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		101	100	105	99	averages
All except types 2,8	t	27.13	57.19	42,29	44.74	42.84
	I	523	1215	837	905	870
	FO	26	538	195	43	201
All except types 3,4	t	34.14	77.52	56.42	53.99	55.52
	I	619	1599	1095	1027	1085
	FO	26	609	195	46	219
All except types 3,5	t	35.75	80.88	55.99	54.09	56.68
	I	619	1523	1015	1013	1043
	FO	26	610	199	43	220
All except types 3,7	t	35.90	83.21	56.54	56.04	57.92
	I	693	1699	1117	1099	1152
	FO	28	714	215	43	250
All except types 3,8	t	34.92	77.04	52.98	54.31	54.82
	I	637	1559	1027	1063	1072
	FO	28	622	197	45	223
All except types 4,5	t	25.54	56.84	46.84	43.97	43.30
	I	517	1251	935	863	892
	FO	26	524	197	44	198

(continued from the previous page)

Table A16. Three variable.six NOR-AND gate design.
(All-interconnection formulation.)
(continued)

Functions numbered after [1]		101	100	105	99	averages
All	t	26.65	60.25	45.02	43.89	43.95
except	I	587	1399	1021	993	1000
types 4,7	FO	26	602	209	46	221
All	t	26.24	56.94	42.61	43.08	42.22
except	I	523	1267	931	913	909
types 4,8	FO	26	538	195	46	202
All	t	26.14	57.39	40.28	42.36	41.54
except	I	543	1289	877	903	903
types 5,7	FO	26	582	199	41	212
All	t	26.62	55.07	39.71	42.44	40.96
except	I	533	1231	853	911	882
types 5,8	FO	26	544	199	45	204
All	t	26.02	58.15	39.98	42.19	41.58
except	I	567	1329	885	953	934
types 7,8	FO	28	610	199	45	221

(continued from the previous page)

Table A16. Three variable.six NOR-AND gate design.
(All-interconnection formulation.)

APPENDIX B

VARIATION OF SUBSCRIPTS IN ACTUAL IMPLEMENTATION OF THE TRIANGULAR INEQUALITIES

In the all-interconnection program, ILLODIE-AIF, when used for NOR-AND and NOR-NAND design cases, the actual range of the subscripts is as follows:

$$i = 1,2,\ldots, R-1$$

$$j = 1,2,\ldots, R-1$$

$$k = 1,2,\ldots, R$$

while for the NOR and AND-OR designs they are

$$i = 1,2,\ldots, R$$

$$j = 1,2,\ldots, R$$

$$k = 1,2,\ldots, R$$

The reasons for choosing different ranges for the NOR-AND and NOR-NAND designs is that only single output networks have been considered for these designs and the additional inequalities generated for the cases where G_i or G_j is the output gate were assumed to be not too effective in reducing the execution time.

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In logical design of optimal networks by integer programming, additional inequalities are added in order to speed-up the computations time. The effects of different types of these additional inequalities for several logical design cases is studied.

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